
CS2501 Schematic and Layout Guidelines

Introduction

This document describes the schematic and layout guidelines for the CS2501 Fractional-N Clock Multiplier.

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1 General Board Considerations

- Use controlled 50Ω characteristic impedance for digital signals unless stated otherwise.

2 Layout Guidelines

2.1 Note 1: Device Decoupling

- Place VDD decoupling capacitors close to device on same side of PCB.

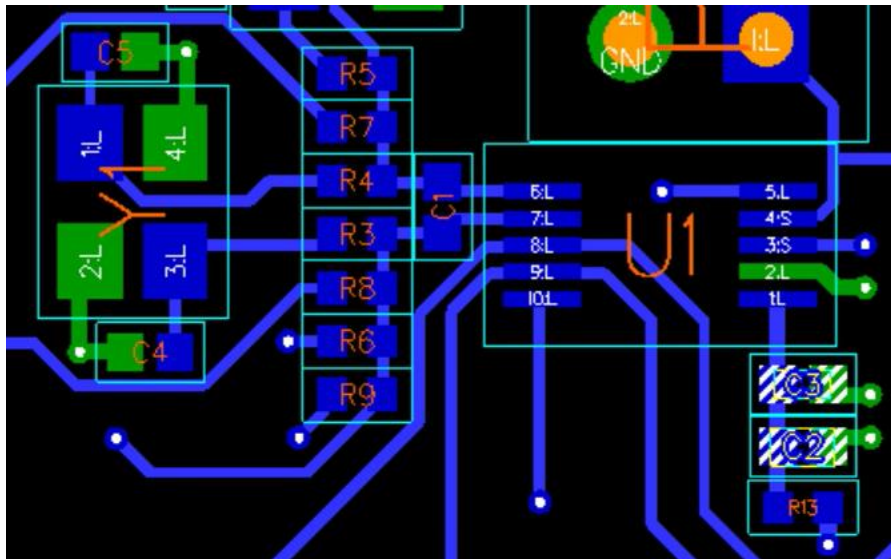


Figure 1 - Device decoupling with VDD decoupling highlighted

2.2 Note 3: Crystal and crystal capacitors

- Place crystal and crystal capacitors close to device on same side of PCB.
- Note that R3 and C1 are not required on a production PCB with CS2501.

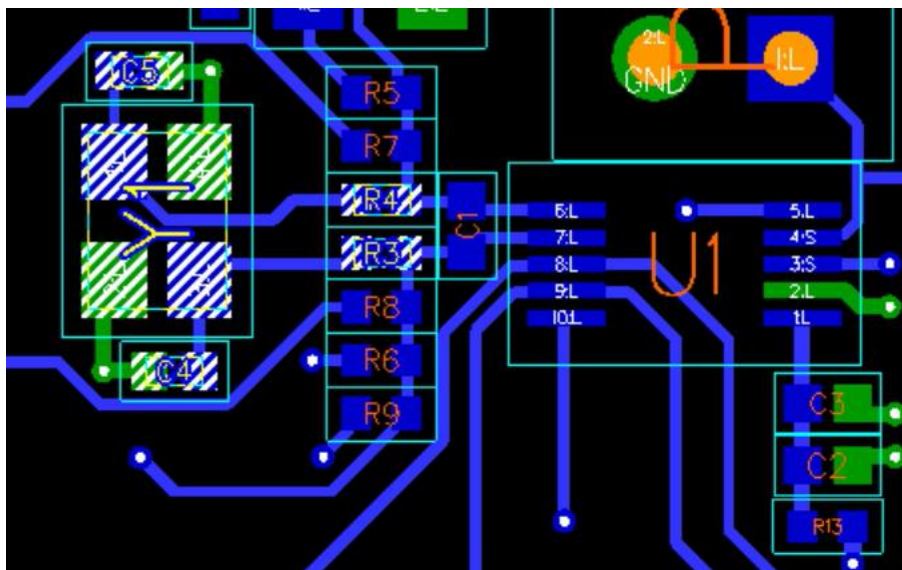


Figure 2 - Crystal and crystal capacitors highlighted

3 Revision History

Revision History	
Revision	Changes
1.0 SEP 2024	Initial version.

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